UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,458	09/28/2001	Hong Wang	42390P11705	5276

7590 08/17/2004

Blakely, Sokoloff, Taylor & Zafman
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, CA 90025-1030

EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2122	

DATE MAILED: 08/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,458	WANG ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending and have been examined. The priority date considered for the application is June 28, 2001.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-30 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-30 of copending Application No. 09/967,220. Although the conflicting claims are not identical, they are not

patentably distinct from each other because both sets of claims recite methods and apparatuses for monitoring events with regard to dynamic optimization of program execution.

For example, claims 1-3 and 8 of the instant application and claims 21-23 of Application No. 09/967,220 both recite microarchitecture event monitors that capture profiles to be processed for dynamic optimization and monitor control vectors with control, handler and trigger fields. Instant claims 4, 5 and 7 and claims 25-27 of 09/927,220 both recite the two-level buffer for storing the captured profiles. Claims 10-12, 17 and 18 of the instant application are analogous to the above, and further recite the limitations to the buffer added by claims 28 and 29 of 09/927,220. Likewise, claims 21-24, 26, and 28-30 of the instant application and claims 1-9 of 09/927,220 recite similar limitations in the form of a method. Claims 11-19 of 09/927,220 recite the same method embodied in a machine-readable medium.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

4. Claims 7-9 are objected to because of the following informalities: The claims further limit the "event monitoring apparatus" of each parent claim, but parent claims 1 and 5 are directed instead to an "event monitoring component." Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, 4-17, 21, 22 and 24-30 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 6,134,710 to Levine et al. (hereinafter "Levine").

With respect to claim 1, Levine discloses an event monitoring component for dynamic optimization (see the abstract) comprising:

(a) an event monitor to selectively capture profiles of one or more microarchitecture events occurring in the execution of an application by a microprocessor based upon configuration information supplied by a software component (see column 7, line 59 to column 8, line 11, which shows a performance monitor for capturing events during execution, and column 8, lines 14-16, which shows that the monitor is controlled or configured by software); and

(b) an interface through which the software component provides the configuration information to direct the operation of the event monitor (see column 8, lines 16-22, which shows an interface for configuring the operation of the monitor).

With respect to claim 2, Levine further discloses one or more monitor control vectors, the monitor control vectors storing the configuration information provided by the software component (see FIGS. 3A and 3B, which show monitor control registers or vectors for storing the configuration),

With respect to claim 4, Levine further discloses a profile buffer to store the captured profiles of the one or more microarchitecture events (see column 11, lines 34-48, which shows a buffer for storing profiles of the events).

With respect to claim 5, Levine further discloses the limitation wherein the profile buffer comprises a first level buffer for initial storage of the captured profiles of the one or more microarchitecture events and a second level buffer for subsequent storage of the captured profiles of the one or more microarchitecture events (see column 10, line 63 to column 11, line 3, which shows storing the profile data in sampled instruction and data address registers, i.e. a first level buffer, and subsequently copying the data to tables in memory, i.e. a second level buffer).

With respect to claim 6, Levine further discloses the limitation wherein the first level buffer is a register file (see the registers of the first level buffer 530 and 540 in FIG. 7).

With respect to claim 7, Levine further discloses the limitation wherein the second level buffer is a memory buffer that is architecturally visible to the software component (see column 11, lines 45-53, which shows that the second level buffer in memory is accessible by and thus architecturally visible to the software).

With respect to claim 8, Levine further discloses the limitation wherein the captured event profiles of each monitored microarchitecture event are made available to a handler routine selected by the software component for processing (see column 11, lines 37-42 and 53-56, which shows that the profile data of each event is made available for processing).

With respect to claim 9, Levine further discloses the limitation wherein the event monitoring apparatus initiates an interrupt or special event handler to notify the software component when captured event profiles are available for processing (see column 10, line 63 to column 11, line 3, which shows signaling an interrupt when profile data is available).

With respect to claim 10, Levine discloses a microprocessor (see FIG. 1 and column 6, lines 57-61), comprising:

(a) an execution pipeline (see the execution units in FIG. 2 and the pipelined instruction cycle 14 in FIG. 4);

(b) one or more event monitors coupled to the execution pipeline to selectively monitor one or more microarchitecture events in the execution of a program and to capture event profiles (see column 7, line 59 to column 8, line 11, which shows performance monitors for capturing events during execution);

(c) one or more monitor control vectors to store configuration information provided by a software component in connection with the operation of the one or more event monitors (see column 8, lines 14-22, which shows monitor control registers or vectors for controlling or configuring the monitors by software); and

(d) a profile buffer to store captured microarchitecture event profiles (see column 11, lines 34-48, which shows a buffer for storing profiles of the events).

With respect to claim 11, Levine further discloses the limitation wherein the captured profiles of the one or more microarchitecture events stored in the buffer are made available to a handler routine selected by the software component for optimization processing (see column 11,

lines 37-42 and 53-56, which shows that the profile data of each event is made available for processing, and column 12, lines 1-6, which shows that the processing is for optimization).

With respect to claim 12, the limitations recited in the claim are analogous to those of claim 5 (see the rationale applied to claim 5 above).

With respect to claim 13, the limitations recited in the claim are analogous to those of claim 6 (see the rationale applied to claim 6 above).

With respect to claim 14, the limitations recited in the claim are analogous to those of claim 7 (see the rationale applied to claim 7 above).

With respect to claim 15, Levine further discloses the limitation wherein the first level buffer is comprised of a plurality of register frames and the second level buffer is comprised of a plurality of memory buffers, with one of the frames of the first level buffer and one of the memory buffers in the second level buffer being assigned to each monitored microarchitecture event (see column 10, line 63 to column 11, line 3, which shows that the first level buffer is comprised of a plurality of registers and that the second level buffer is comprised of a plurality of tables in memory, and column 8, lines 24-35, which shows that the buffers are employed and thus assigned for each selected or monitored event).

With respect to claim 16, Levine further discloses the limitation wherein the profiles of a microarchitecture event stored in a frame assigned to the microarchitecture event in the first level buffer memory are spilled into a buffer assigned to the microarchitecture event in the second level memory buffer when the frame assigned to the microarchitecture event in the first level

memory buffer is fully allocated or when a condition established by the software component is met (see column 10, line 63 to column 11, line 3, which shows copying or spilling the contents of the first level buffer to the second level buffer when an interrupt is serviced or met, and column 8, lines 24-35, which shows establishing the condition for the interrupt).

With respect to claim 17, Levine further discloses the limitation wherein the captured profiles of a microarchitecture event are made available to the handler routine when the buffer assigned to the event in the second level memory buffer is fully allocated or when a condition established by the software component is met (see column 11, lines 37-42 and 53-56, which shows that the profile data of each event is made available for processing when an interrupt is serviced or met, and column 8, lines 24-35, which shows establishing the condition for the interrupt).

With respect to claim 21, Levine discloses a method (see the abstract) comprising:

(a) receiving configuration information from a software component directing the monitoring of one or more microarchitecture events connected with the operation of a microprocessor in executing an application (see column 8, lines 14-22, which shows software for controlling or configuring the monitoring of events);

(b) monitoring the one or more microarchitecture events and capturing profiles of the one or more microarchitecture events (see column 7, line 59 to column 8, line 11, which shows performance monitors for capturing the events during execution);

(c) storing the captured event profiles in a profile buffer (see column 11, lines 34-48, which shows a buffer for storing profiles of the events); and

(d) making the profiles of the event available to the software component for optimization processing (see column 11, lines 37-42 and 53-56, which shows that the profile data of each event is made available for processing, and column 12, lines 1-6, which shows that the processing is for optimization).

With respect to claim 22, Levine further discloses the limitation wherein receiving the configuration information from the software component comprises receiving information regarding the setting of one or more monitor control vectors (see FIGS. 3A and 3B, which show monitor control registers or vectors for storing the configuration).

With respect to claim 24, the limitations recited in the claim are analogous to those of claim 5 (see the rationale applied to claim 5 above).

With respect to claim 25, the limitations recited in the claim are analogous to those of claim 6 (see the rationale applied to claim 6 above).

With respect to claim 26, the limitations recited in the claim are analogous to those of claim 7 (see the rationale applied to claim 7 above).

With respect to claim 27, Levine further discloses assigning a register in the first stage and a memory buffer in the second stage to each monitored microarchitecture event (see column 8, lines 24-35, which shows that the buffers are employed and thus assigned for each selected or monitored event).

With respect to claim 28, Levine further discloses storing the profiles of each monitored microarchitecture event in the register assigned to the microarchitecture event in the first stage as the profiles of the microarchitecture event are captured (see column 10, line 63 to column 11, line 3, which shows storing the profile data in the first stage when it is captured).

With respect to claim 29, Levine further discloses spilling the profiles of a microarchitecture event from the register assigned to the microarchitecture event in the first stage to the memory buffer assigned to the microarchitecture event in the second stage when the register is fully allocated or when a condition established by the software component is met (see column 10, line 63 to column 11, line 3, which shows copying or spilling the contents of the first stage to the second stage when an interrupt is serviced or met, and column 8, lines 24-35, which shows establishing the condition for the interrupt).

With respect to claim 30, Levine further discloses notifying the software component when the register assigned to the event in the second stage of the memory buffer is fully allocated or when a condition established by the software component is met (see column 10, line 63 to column 11, line 3, which shows signaling an interrupt to notify the software, and column 8, lines 24-35, which shows establishing the condition for the interrupt).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3, 18-20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levine, as applied to claims 2, 10 and 22 above, respectively.

With respect to claim 3, Levine further discloses the limitation wherein each monitor control vector includes:

(a) a control field to specify a microarchitecture event to monitor (see column 8, lines 44-52, which shows a control field for selecting events to monitor); and

(c) a trigger field to specify when the microarchitecture event is monitored (see column 8, lines 36-44, which shows a threshold field or trigger field for specifying when to count or monitor events).

Although Levine further discloses that the monitor control register or vector includes an interrupt field for enabling a handler routine to process the profiles of the event (see interrupt handling routine 580 in FIG. 7 and column 8, lines 24-35), Levine does not expressly disclose the limitation wherein each monitor control vector includes:

(b) a handler field, the handler field containing a pointer to a handler routine to process the profiles of the microarchitecture event.

However, the system of Levine inherently includes such a pointer. The address of the handler routine must be known in order to service the interrupt and process the profiles of the event (see column 10, line 63 to column 11, line 3). The address or pointer may be stored, for example, as a field within a control register or vector.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store a pointer to the handler routine taught by Levine in a handler field of the monitor control registers or vectors, similarly to the interrupt field taught also by Levine, for the purpose of providing the address with which to invoke the routine.

With respect to claim 18, the limitations recited in the claim are analogous to those of claim 3 (see the rationale applied to claim 3 above).

With respect to claim 19, although Levine further discloses that the events are monitored during pipelined execution (see column 6, lines 4-12), Levine does not expressly disclose the limitation wherein the one or more microarchitecture events are monitored during an exception detection stage of the execution pipeline.

However, the system of Levine inherently detects exceptions. Exceptions, such as interrupts, must be detected in order to be handled (see interrupt handling routine 580 in FIG. 7). Any stage in the pipelined instruction cycle may comprise exception detection, such as the execute instruction stage (see FIG. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to monitor events during a stage of the execution pipeline, as taught by Levine, such as during an exception detection stage.

With respect to claim 20, although Levine further discloses that the events are monitored during pipelined execution (see column 6, lines 4-12) and that the profiles are stored in a buffer (see column 11, lines 34-48), Levine does not expressly disclose the limitation wherein the

captured microarchitecture event profiles are stored in the memory buffer during a write back stage of the execution pipeline.

However, the system of Levine includes a load/store unit for reading and writing to memory (see FIG. 2). Writing back to memory may occur, for example, during the complete instruction stage of the pipelined instruction cycle (see FIG. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the profiles in the memory buffer, as taught by Levine, during a stage of the execution pipeline that includes a write back stage, such as during the complete instruction stage.

With respect to claim 23, the limitations recited in the claim are analogous to those of claim 3 (see the rationale applied to claim 3 above).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. U.S. Pat. No. 6,549,930 to Chrysos et al. discloses hardware event monitors for collecting profile information from instructions in an execution pipeline and software for processing the profiles to direct optimization (see column 7, lines 10-43). U.S. Pat. No. 5,996,092 to Augsburg et al. discloses a hardware and software system for monitoring program execution using a trace buffer (see the abstract and FIGS. 1 and 9). U.S. Pat. No. 6,375,367 to Dean et al. discloses an apparatus and method for monitoring a computer system to guide optimization (see the title).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy

TUAN DAM
SUPERVISORY PATENT EXAMINER